Atty. Docket No. OPP031058US
Serial No: 10/736,063

Remarks

Applicant and his representatives wish to thank Examiner Mitchell for the thorough examination of the present application, the clear explanations in the Final Office Action dated February 8, 2006, and for the very helpful and courteous discussion held with their undersigned representative on March 31, 2006. Applicant's undersigned representative thanks Examiner Mitchell and the USPTO for identifying the correct application number in the previous amendment and matching the previous amendment with the correct application, thereby saving Applicant from a possible inadvertent abandonment of the application. Claim 1 has been amended as discussed to recite forming a trench in the substrate and also to recite selectively etching a sacrificial layer to form a sidewall opening over an area of the semiconductor substrate ***including the trench***. The following remarks shall further summarize and expand upon topics discussed.

Claims 1, 3-7, and 9-12 have been amended. Claim 13 has been canceled. Claims 14-21 have been added. Therefore, Claims 1-12 and 14-21 are active in this application. No new matter is introduced by the present Amendment.

The present invention relates to a method of forming a gate in a semiconductor device comprising the steps of:

a) forming a trench in a semiconductor substrate;

b) forming a gate oxide layer on the semiconductor substrate;

c) forming on the semiconductor substrate a sacrificial layer;

d) selectively etching the sacrificial layer to form a sidewall opening over an area of the semiconductor substrate including the trench;

e) forming a polycrystalline silicon layer on an area of the gate oxide layer exposed through the sidewall opening and on the sacrificial layer;

f) anisotropically etching the polycrystalline silicon layer such that sidewall gates remain on sidewalls of the sidewall opening; and

g) removing the sacrificial layer.

The cited references do not disclose or suggest, alone or taken together, a method including selectively etching the sacrificial layer to form a sidewall opening over an area of a semiconductor substrate including a trench (see step d above). Thus, the present claims are patentable over the cited references.

The Rejection of Claims 1-2, 5-8, and 11-13 under 35 U.S.C. § 102(e)

The rejection of Claims 1-2, 5-8, and 11-13 under 35 U.S.C. § 102(e) as being anticipated by Lin et al. (US 6,734,055, hereinafter "Lin") is respectfully traversed.

The method of Claim 1 is exemplified by forming a trench 10 in a substrate 11 (see paragraph [0011] and FIG. 1a), forming a sacrificial layer 13 (see paragraph [0011] and FIG. 1a), and etching the sacrificial layer 13 to form a sidewall opening over an area of a semiconductor substrate 11 comprising the trench 10 (see paragraph [0014] and FIG. 1b).

Lin discloses a method that includes forming shallow trench isolation 110, forming and patterning nitride layer 130 to form gate opening 140 over the substrate 100 (see col. 5, ll. 4-9, and FIG. 2a). Nitride layer 130 remains over shallow trench isolation 110 after formation of the gate opening 140 (see col. 5, ll. 4-9, and FIG. 2a). Thus, Lin fails to disclose selectively etching a sacrificial layer to form a sidewall opening over an area of a semiconductor substrate including a trench, as recited in Claim 1. Therefore, Lin fails to anticipate the method of Claim 1, and the rejection of Claim 1 under 35 U.S.C. § 102(e) should be withdrawn.

Claims 2, 5-8, and 11-12 depend from Claim 1, and thus include all of the limitations of Claim 1. Therefore, Claims 2, 5-8, and 11-12 are patentable over Lin for essentially the same reasons as Claim 1.

Claim 13 has been canceled. Thus, the rejection under 35 U.S.C. § 102(e) has been obviated and should be withdrawn.

The Rejection of Claims 3-4 and 9-10 under 35 U.S.C. § 103(a)

The rejection of Claims 3-4 and 9-10 under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of Burns et al. (US 6,258,679, hereinafter "Burns") is respectfully traversed.

As explained above, Lin is deficient with regard to etching a sacrificial layer to form a sidewall opening over an area of a semiconductor substrate including the trench, as recited in Claim 1.

Burns makes no mention of a trench in the substrate 10, and thus also fails to disclose etching a sacrificial layer to form a sidewall opening over an area of a semiconductor substrate including a trench, as recited in Claim 1. As a result, Burns cannot cure the deficiencies of Lin with regard to the presently claimed process. Therefore, the method of Claim 1 cannot be rendered obvious by Lin in view of Burns, and the rejection of Claim 1 under 35 U.S.C. § 103(a) should be withdrawn.

Claims 3-4 and 9-10 depend from Claim 1, and thus include all of the limitations of Claim 1. Therefore, Claims 3-4 and 9-10 are patentable over Lin in view of Burns for essentially the same reasons as Claim 1.

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Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

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